IN THE CLAIMS

Please amend claims 7, 10 and 14 and cancel claims 9 and 15 in accordance with the following listing showing the status of all claims in the application.

1. (Previously Presented) A circuit comprising:

a first circuit having a first input and a first output, wherein said first output includes a function of a signal at said first input and also includes a first noise component resulting from noise experienced by said first circuit;

a second circuit, located proximal to said first circuit and having a second input and a second output, wherein said second output includes a function of a signal at said second input and also includes a second noise component resulting from noise experienced by said second circuit, and wherein the second noise component is approximately equal to the first noise component;

a subtractor circuit connected to said first circuit and to said second circuit to subtract said second output from said first output; and

a digital circuit located proximate to said first circuit and to said second circuit.

2. (Canceled)

3. (Previously Presented) A circuit according to claim 1, wherein said subtractor circuit further comprises a halving circuit which inputs a signal having an input amplitude and outputs the signal at one-half the input amplitude.

4. (Previously Presented) A circuit comprising:

a first circuit having a first input and a first output, wherein said first output includes a function of a signal at said first input and also includes a first noise component resulting from noise experienced by said first circuit;

a second circuit having a second input and a second output, wherein said second output includes an input signal component which is a function of a signal at said second input and also includes a second noise component resulting from noise experienced by said second circuit, wherein the input signal component is a null output, and wherein the second noise component is approximately equal to the first noise component;

a third circuit having a third input connected to said first output and a fourth input connected to said second output to subtract said second output from said first output; and

a digital circuit proximal to said first circuit and to said second circuit.

5. (Canceled)

6. (Previously Presented) A circuit according to claim 4, wherein said first circuit, said second circuit, said third circuit, and said digital circuit are on a single integrated circuit chip.

7. (Currently Amended) A circuit comprising:

a first circuit having a first input and a first output, wherein said first output includes a function of a signal at said first input and also includes a noise component resulting from noise experienced by said first circuit;

a second circuit having a second input and a second output;

a signal supplying circuit supplying to the second input a signal which is an inverse of the signal at the first input; ~~and~~

a third circuit having a third input connected to said first output and a fourth input connected to said second output, and subtracting said second output from said first output; and

a digital circuit proximal to said first circuit and to said second circuit.

8. (Previously Presented) A circuit according to claim 7 wherein said third circuit further comprises a halving circuit which inputs a signal having an input amplitude and outputs the signal at one-half the input amplitude.

9. (Canceled)

10. (Currently Amended) A circuit according to claim ~~9~~ 7, wherein said first circuit, said second circuit, said third circuit, and said digital circuit are on a single integrated circuit chip.

11. (Previously Presented) An integrated circuit chip (IC) comprising:

a plurality of analog circuits, each proximal to each other, and each of said plurality of analog circuits producing an output signal which includes a function of an input signal and also includes a noise component resulting from noise experienced by said plurality of analog circuits;

a noise separator circuit, proximal to said plurality of analog circuits, and producing a noise signal based on noise experienced by said noise separator circuit, wherein the noise signal is approximately equal to the noise component of the output signal output by each of the plurality of analog circuits; and

a noise canceling circuit which processes said output signals with said noise signal to reduce the noise component of the output signal output by each of the plurality of analog circuits.

12. (Original) An IC according to claim 11 wherein said noise canceling circuit comprises a subtractor circuit.

13. (Previously Presented) An IC according to claim 11 wherein said noise canceling circuit further comprises a halving circuit which inputs a signal having an input amplitude and outputs the signal at one-half the input amplitude.

14. (Currently Amended) A noise cancellation method comprising the steps:

supplying a first signal to a first circuit;

reading a first output from said first circuit;

supplying a signal to a second circuit which results in a null output from the second circuit, wherein said second circuit is located proximal to said first circuit;

reading a second output from said second circuit; and

combining said first output with said second output to produce a combinational output,

wherein a noise component of the first output due to noise experienced by said first circuit is approximately equal to a noise component of the second circuit due to noise experienced by said second circuit, and

wherein said ~~step of combination further comprises the step of inputting a signal having an input amplitude and outputting the signal at one-half the input amplitude~~ second circuit is identical to said first circuit.

15. (Canceled)

16. (Original) A method according to claim 14 wherein said step of combination comprises the step of subtracting said second output from said first output.

17. (Canceled)

18. (Canceled)

19. (Canceled)

20. (Previously Presented) A circuit according to claim 1, wherein said second circuit is identical to said first circuit.

21. (Previously Presented) A circuit according to claim 1, wherein the noise experienced by said first circuit and said second circuit is electromagnetic environmental noise.

22. (Previously Presented) A circuit according to claim 1 wherein said second circuit is located close enough to said first circuit so that said second circuit experiences approximately the same noise as said first circuit.

23. (Previously Presented) A circuit according to claim 1, wherein said subtractor circuit is digital.

24. (Previously Presented) A circuit according to claim 1, wherein said subtractor circuit is analog.

25. (Previously Presented) A circuit according to claim 4, wherein said second circuit is identical to said first circuit.

26. (Previously Presented) A circuit according to claim 4, wherein the noise experienced by said first circuit and said second circuit is electromagnetic environmental noise.

27. (Previously Presented) A circuit according to claim 7, wherein said second circuit is identical to said first circuit.

28. (Previously Presented) A circuit according to claim 11, wherein the noise experienced by said plurality of analog circuits and said noise separator circuit is electromagnetic environmental noise.

29. (Previously Presented) A circuit according to claim 14, wherein the noise experienced by said first circuit and said second circuit is electromagnetic environmental noise.